IN THE CLAIMS:

1. (Currently Amended) A method of impedance control, comprising:

providing an input/output cell having a controllable input/output impedance;

providing a reference cell including a node having a variable voltage;

comparing the voltage of the node to a reference voltage;

adjusting the voltage of the node during a defined period and according to a defined procedure, including the step of, during said defined period, activating a number of resistance devices to adjust the voltage of the node until the voltage of the node becomes within a given range of the reference voltage;

during said defined period, generating a digital signal representing the number of resistance devices activated during said period; and

transmitting the digital signal to the input/output cell to adjust the input/output impedance.

2. (Original) A method according to Claim 1, wherein:

the generating step includes the step of increasing a count value during said defined period; and

the transmitting step includes the step of transmitting said count value to the input/output cell after the defined period.

3. (Original) A method according to Claim 2, wherein:

the reference cell includes a series of transistors for adjusting the voltage of the node; and

the adjusting step includes the step of using the count value to activate said transistors in a given order to adjust the voltage of the node.

4. (Original) A method according to Claim 1, wherein:

the reference cell includes a first set of transistors for adjusting the voltage of the node;

the input/output cell includes a second set of transistors for adjusting the input/output impedance;

each of the transistors of said first set is associated with one of the transistors in said second set;

the adjusting step includes the step of activating a subset of the first set of transistors to adjust the voltage of said node; and

the transmitting step includes the step of transmitting the digital signal to the input/output cell to activate transistors of the second set of transistors that are associated with said subset of the first set of transistors.

5. (Original) A method according to Claim 1, wherein:

the input/output impedance of the input/output cell varies in a defined manner as a function of a given set of variables; and

the variable voltage of the node of the reference cell also varies in said defined manner as a function of said given set of variables.

6. (Original) A method according to Claim 5, wherein:

the reference cell includes a reference resistor for establishing the variable voltage at said node; and

said resistor has an impedance that varies in said defined manner as a function of said given set of variables.

7. (Original) A method according to Claim 1, wherein the adjusting step includes the steps of:

if the voltage of the node is less than the reference voltage, then increasing the voltage of the node in a first manner; and

if the voltage of the node is more than the reference voltage, then decreasing the voltage of the node in a second manner.

8. (Original) A method according to Claim 7, wherein:

the increasing step includes the steps of

i) applying a first signal to a digital controller, and

ii) the digital controller applying a signal to the reference cell to increase the voltage of the node;

the decreasing step includes the steps of

i) applying a second signal to the digital controller, and

ii) the digital controller applying a signal to the reference cell to decrease the voltage of the node; and

the generating step includes the step of using the digital controller to generate the digital signal.

9. (Currently Amended) A circuit for controlling the impedance of an input/output cell having a varying input/output impedance, said circuit comprising:

a node having a variable voltage;

a comparator for comparing the voltage of the node to a reference voltage;

means for adjusting the voltage of the node during a defined period and according to a defined procedure, including means for activating a number of resistance devices during said defined period to adjust the voltage of the node until the voltage of the node becomes within a given range of the reference voltage ;

a digital generator for generating a digital signal representing the number of resistance devices activated during said defined period; and

means for transmitting the digital signal to the input/output cell to adjust the input/output impedance.

10. (Original) A circuit according to Claim 9, wherein:

the digital generator increases a count value during said defined period; and

the transmitting means transmits said count value to the input/output cell after the defined period.

11. (Original) A circuit according to Claim 10, wherein the adjusting means includes:

a series of transistors for adjusting the voltage of the node; and

means for using the count value to activate said transistors in a given order to adjust the voltage of the node.

12. (Original) A circuit according to Claim 9, wherein:

the input/output cell includes a first set of transistors for adjusting the input/output impedance;

the circuit further includes a second set of transistors for adjusting the voltage of the node;

each of the transistors of said second set is associated with one of the transistors in said first set;

the adjusting means includes means for activating a subset of the second set of transistors to adjust the voltage of said node; and

the transmitting means includes means for transmitting the digital signal to the input/output cell to activate transistors of the first set of transistors that are associated with said subset of the second set of transistors.

13. (Original) A circuit according to Claim 9, wherein:

the input/output impedance of the input/output cell varies in a defined manner as a function of a given set of variables; and

the variable voltage of said node also varies in said defined manner as a function of said given set of variables.

14. (Original) A circuit according to Claim 13, wherein:

the circuit further includes a reference resistor for establishing the variable voltage at said node; and

said resistor has an impedance that varies in said defined manner as a function of said given set of variables.

15. (Original) A circuit according to Claim 9, wherein the adjusting means includes:

means for increasing the voltage of the node in a first manner if the voltage of the node is less than the reference voltage; and

means for decreasing the voltage of the node in a second manner if the voltage of the node is more than the reference voltage.

16. (Original) A circuit according to Claim 9, wherein said circuit is a digital controller designed as a synthesized core or macro.